Remarks

In the Office action mailed September 9, 2004, claims 1-4, 13, 19, and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,446,567 ("Iida et al."). See Office action at 2. In addition, claims 5-12, 21, and 22 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. See id. at 2. Claims 14-18 were allowed. These rejections and objections will be discussed below.

Applicants contend that rejected claims 1-4, 13, 19, and 20 are not anticipated by Iida et al. In order to anticipate a claim, a reference must teach all the elements of a claim. See Verdegaal Bros., Inc. v. Union Oil Co., 814 F.2d 628, 631 (Fed. Cir. 1987). Iida et al. does not teach all the elements of rejected independent claims 1 and 19. Therefore, these independent claims and each of their dependent claims are not anticipated by Iida et al.

Claim 1

Applicants' claim 1 is directed to a shift register device. See Application, claim 1. The claimed shift register device comprises:

> a bit data input line along which bit data is to be shifted toward an output terminal;
>
> latches in succession connected in series along said bit data input line and disposed between an input terminal and said output terminal, each latch capable of storing one bit of data;
>
> transistor pass gates; and
>
> control signal input lines connected to said transistor pass gates, each control signal input line operable to provide a control signal to one of said transistor pass gates to shift bit data to and from said latches along said bit data input line,

> wherein said control signals are applied in a staggered time pattern. Id.

Applicants assert that Iida et al. does not teach at least two elements of claim 1: 1) latches in succession connected in series along said bit data input line; and 2) control signal input lines providing a control signal to one of the transistor pass gates to shift bit data to and from latches along the bit data input line, wherein the control signals are applied in a staggered time pattern. See id.

Iida et al. does not teach a shift register circuit employing latches. Instead, Iida et al.'s shift register circuit comprises, in part, two transfer gate circuits, an inverter circuit, and a signal follower circuit. See Iida et al., col. 1, ln. 29-48. According to the Office action, Iida et al.'s inverter circuit (12) and signal follower circuit (14) are latches "insofar as a latch is a device which holds the last value of its input until enabled to acquire a new value." Office action at 2. A latch also may be defined as "a bistable storage device . . . that can reside in either of two states by virtue of a feedback arrangement, in which the outputs are connected back to the opposite inputs." T.L. Floyd, Digital Fundamentals 389 (6th ed., 1997). (Copy submitted with Response) Using either the Office action's definition or the definition provided by Applicants, Iida et al.'s inverter circuit 12 and signal follower circuit (14) are not latches since neither of these circuits is capable of holding the last value of their inputs as there is no feedback loop in which the outputs are connected back to the opposite inputs. Iida et al. notes the following about signal follower circuit 14:

> The circuit 14 is so designed as to follow a signal which the transfer gas [sic] circuit 11 generates when it is on. That is, the level of the output signal of the circuit 14 changes according to the level of the output signal of the transfer gate circuit 11 when it is on. While the

> transfer gate circuit is off, the output signal of the circuit 14 is held at a reference potential, i.e. ground potential. Iida et al., col. 2, ln. 8-15.

Iida et al.'s inverter circuit 12 inverts the signal provided to it by the first transfer gate circuit. See id., col. 1, ln. 66-68. Neither the inverter circuit nor the signal follower circuit maintain the previous value of the input and their output is dependent only on the present input. In contrast, Applicants' latches' output is dependent on the present input and the stored value, since the stored value of each latch may be shifted either to another latch or to a position external to the latches upon application of the control signal. See Application, pp. 3-4, ln. 29-10; see id., claim 4. Iida et al.'s inverter circuit and signal follower circuit are not latches, nor are they the equivalents of latches. Since Iida et al. does not teach the latches in Applicants' claim 1, this claim is not anticipated.

Iida et al. also fails to teach Applicants' claimed control signal input lines providing a control signal to one of the transistor pass gates to shift bit data to and from latches along the bit data input line, wherein the control signals are applied in a staggered time pattern. As noted above, Iida et al. fails to teach latches. Therefore, Iida et al. also fails to teach control signal input lines which provide a control signal to shift data to and from latches. Iida et al. does not teach this element of Applicants' claim 1 and therefore the claim is not anticipated by Iida et al.

Further, even if Iida et al. did teach latches, the reference does not teach control signals applied in a staggered time pattern. The Office action assumes that "staggered," as used in the claim means that "each positive pulse is applied one at a time." See Office action at 2. Applicants respectfully point out that "staggered" as used in the specification and claims means that control signals are applied at different points in time. See Application, pp. 6-

7, ln 33-1. This is illustrated by Applicants' Fig. 4, which shows control signals S_1, S_2, S_3, and S_4 being applied at times P_1, P_2, P_3, and P_4, respectively. See id., Fig. 4. The staggered control signals cause a data bit stored in each latch element to be transferred to the next latch element or an output before another data bit from an input or a preceding latch element over-writes the existing data bit. This staggering pattern is not taught by Iida et al. Figs. 3a and 3b of Iida et al. show that the two clock signals are not applied at different points in time as the control signals are in claim 1. See Iida et al., Figs. 3a and 3b. Therefore, since Iida et al. does not teach control signals applied in a staggered time pattern, Iida et al. does not anticipate Applicants' claim 1. Indeed, since the inverter and follower circuitry do not store data, Applicants' reason for staggered control would not be suggested by Iida et al.'s cicuit.

Claims 2-13

Claims 2-13 are dependent claims of independent claim 1. As noted above, independent claim 1 is not anticipated by Iida et al. Therefore, dependent claims 2-13 are novel for at least the same reasons that claim 1 is novel.

Claim 19

Applicants' independent claim 19, like independent claim 1, is also directed to a shift register device. See Application, claim 19. Specifically, Applicants' claimed shift register device comprises:

> latches in succession and connected in series along a bit data input line, each latch storing one bit of data; and
>
> control signal input lines in succession connected to said latches, each line operable to provide a control signal to shift bit data along said bit data input line, wherein said control signals are applied in a staggered time pattern and in reverse succession. See Application, claim 19.

Applicants assert claim 19 is novel because, as shown above, Iida et al. does not teach latches. Further, since Iida et al. does not teach latches, it also does not teach control signal input lines in succession connected to said latches. Finally, as shown above, Iida et al. does not teach control signals applied in a staggered time pattern. Since Iida et al. fails to teach any of these elements of Applicants' claim 19, claim 19 is novel.

Claims 20-22

Claims 20-22 are dependent claims of Applicants' independent claim 19. Applicants have shown claim 19 is novel. Therefore, dependent claims 20-22 are also novel for at least the same reasons that claim 19 is novel.

Objections

As noted above, claims 5-12, 21, and 22 were objected to in the Office action as being dependent on a rejected base claim (i.e., claims 1 or 19). See Office action at 2. Applicants thank the Examiner for the indication of allowability of the subject matter recited in these claims. However, Applicants decline to rewrite these claims into independent form in light of the arguments made above as to the patentability of the independent claims 1 and 19. Applicants believe these objections have been addressed by the above showing that independent claims 1 and 19 are novel. Therefore, claims 5-12, 21, and 22 are not dependent on a rejected base claim. Applicants request the withdrawal of the objections to these claims.

Conclusion

Applicants have shown claims 1-13 and claims 19-22 are not anticipated by the cited reference. Applicants therefore request a Notice of Allowance for all the claims in the Application.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signed: Sally Azevedo
Typed Name: Sally Azevedo

Date: December 6, 2004

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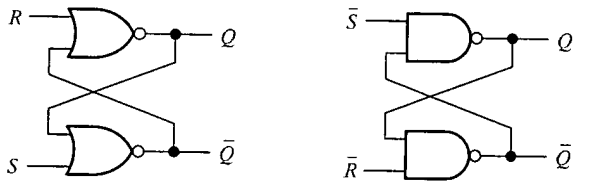
8–1 ■ LATCHES

The latch is a type of bistable storage device that is normally placed in a category separate from that of flip-flops. Latches are basically similar to flip-flops because they are bistable devices that can reside in either of two states by virtue of a feedback arrangement, in which the outputs are connected back to the opposite inputs. The main difference between latches and flip-flops is in the method used for changing their state. After completing this section, you should be able to

☐ Explain the operation of a basic S-R latch ☐ Explain the operation of a gated S-R latch ☐ Explain the operation of a gated D latch ☐ Implement an S-R or D latch with logic gates ☐ Describe the 74LS279 and 74LS75 quad latches

The S-R Latch

A **latch** is a type of **bistable** multivibrator. An active-HIGH input S-R (SET-RESET) latch is formed with two cross-coupled NOR gates as shown in Figure 8–1(a); an active-LOW input $\overline{S}$-$\overline{R}$ latch is formed with two cross-coupled NAND gates as shown in Figure 8–1(b). Notice that the output of each gate is connected to an input of the opposite gate. This produces the regenerative **feedback** that is characteristic of all **multivibrators.**



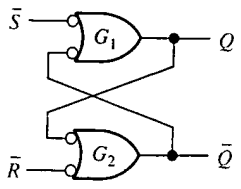
(a) Active-HIGH input S-R latch (b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

FIGURE 8–1
Two versions of SET-RESET (S-R) latches.

To understand the operation of the latch, we will use the NAND gate $\overline{S}$-$\overline{R}$ latch in Figure 8–1(b). This latch is redrawn in Figure 8–2 with the negative-OR equivalents used for the NAND gates. This is done because LOWs on the $\overline{S}$ and $\overline{R}$ lines are the activating inputs.

The latch in Figure 8–2 has two inputs, $\overline{S}$ and $\overline{R}$, and two outputs, Q and $\overline{Q}$. Let's start by assuming that both inputs and the Q output are HIGH. Since the Q output is connected back to an input of gate G_2, and the $\overline{R}$ input is HIGH, the output of G_2 must be LOW. This LOW output is coupled back to an input of gate G_1, ensuring that its output is HIGH.

FIGURE 8–2
Negative-OR equivalent of the NAND gate $\overline{S}$-$\overline{R}$ latch in Figure 8–1(b).



When the Q output is HIGH, the latch is in the **SET** state. It will remain in this state indefinitely until a LOW is temporarily applied to the $\overline{R}$ input. With a LOW on the $\overline{R}$ input and a HIGH on $\overline{S}$, the output of gate G_2 is forced HIGH. This HIGH on the $\overline{Q}$ output is coupled back to an input of G_1, and since the $\overline{S}$ input is HIGH, the output of G_1 goes LOW. This LOW on the Q output is then coupled back to an input of G_2, ensuring that the $\overline{Q}$ output remains HIGH even when the LOW on the $\overline{R}$ input is removed. When the Q output is